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2188

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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The Application of:

Serge Lasserre

TI-31354

Technology Center 2100

Serial No: 09/932,381

Art Unit: 2188

Filed: August 17, 2001

Examiner: Reginald G. Bragdon

For: Local Memory With Indicator Bits to Support Concurrent DMA and CPU Access

Conf. No.: 4434

INFORMATION DISCLOSURE STATEMENT PURSUANT TO §1.97(c)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(a)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on July 13, 2004.

Robin E. Barnum

Dear Sir:

Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed PTO-1449. Copies of the noted references are enclosed herewith.

Applicant is submitting herewith a copy of a communication from a foreign patent office in a counterpart foreign application and copies of the documents listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This Information Disclosure statement is being submitted before the mailing date of either a Final Action or a Notice of Allowance and the fee set forth in 37 CFR 1.17(p) should be charged to Texas Instruments Incorporated, Deposit Account 20-0668.

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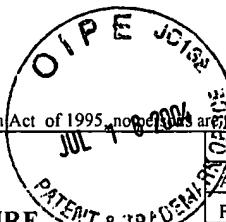
Respectfully submitted,

Robert D. Marshall, Jr.
Attorney for Applicant(s)
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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete If Known

Application Number	
Filing Date	August 17, 2001
First Named Inventor	Serge Lasserre
Group Art Unit	2188
Examiner Name	Reginald G. Bragdon

Sheet

1

of

1

Attorney Docket No.

TI-31354

U.S. PATENT DOCUMENTS

Exam. Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

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CA	IBM Corp.; <i>Use of Dirty, Buffered, and Invalidate Bits for Cache Operations</i> , IBM Technical Disclosure Bulletin; New York, US, vol. 35, no. 1A, 1 June 1992, pg. 124.		
CB	IBM Corp.; <i>Low End Parallel Bus Memory Refresh Activated Bus Timeout Control</i> , IBM Technical Disclosure Bulletin; New York, US, vol. 31, no. 3, 1 August 1988, pgs. 90-92.		
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